

R22

Code No: 183AP

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech II Year I Semester Examinations, February - 2024

DIGITAL ELECTRONICS

(Common to CSE, IT, CSIT, CE(SE), CSE(CS), CSE(DS), CSD)

Time: 3 Hours

Max. Marks: 60

Note: This question paper contains two parts A and B.

i) **Part- A** for 10 marks, ii) **Part - B** for 50 marks.

- Part-A is a compulsory question which consists of ten sub-questions from all units carrying equal marks.
- Part-B consists of **ten questions** (numbered from 2 to 11) **carrying 10 marks each**. From each unit, there are two questions and the student should answer one of them. Hence, the student should answer five questions from Part-B.

PART- A

(10 Marks)

- 1.a) Write the principle of Distributive law. [1]
b) Convert the binary to gray code: 111011_2 [1]
c) Define minterm and Maxterm. Give examples. [1]
d) What is K map? [1]
e) Identify the function of select inputs of a MUX. [1]
f) Compare the function of decoder and encoder. [1]
g) What are the applications of Flip-flops? [1]
h) What are the classifications of sequential circuits? [1]
i) What is the cause for essential Hazard? [1]
j) What is memory decoding? [1]

PART - B

(50 Marks)

- 2.a) Perform the following operations using 2's complement:
i) $1001.11 - 1100.10$ ii) $87 - 99$.
b) Explain the different logic gates in detail. [5+5]

OR

- 3.a) Justify the statement that "Gray code is a class of reflected code".
b) Simplify the Boolean expressions to minimum number of literals:
i) $X' + XY + XZ' + XYZ'$ ii) $(X+Y)(X+Y')$. [4+6]

- 4.a) Realize the basic gates using NAND and NOR gates only.
b) Use tabular method and simplify the function $F = \sum m(2,3,5,6,7,9,12,14,15)$. [5+5]

OR

- 5.a) Simplify the following function and realize using NOR gate:
 $F(A,B,C) = A'BC' + ABC + B'C' + A'B'$
b) Simplify the following Boolean function for minimal SOP form using K-map:
 $F(W,X,Y,Z) = \sum(1,3,7,11,15) + d(0,2,5)$. [5+5]

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- 6.a) Construct a 3*8 decoder using logic gates.
b) Implement the following function using suitable multiplexer:
 $F(A, B, C, D) = \Sigma(1, 3, 4, 11, 12, 13, 14, 15)$. [5+5]

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- 7.a) Design full adder and realize it using two adder and logic gates.
b) Define magnitude comparator and Design a 2-bit comparator to compare two 2-bit numbers. [5+5]

- 8.a) Explain about ripple counter.
b) Design a synchronous counter to generate the sequence 0, 1, 2, 3, 5, 8 and repeat the sequence using T flip-flops. [4+6]

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- 9.a) Design a 4 bit binary synchronous counters with D-flip flop.
b) Compare latch and flip-flop. [5+5]

- 10.a) Explain the following related to sequential circuits with suitable:
i) State diagram ii) State Table iii) State Assignment.

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- b) Give hazard free realization for the following Boolean function:
 $F(A, B, C, D) = \Sigma m(0, 2, 6, 7, 8, 10, 12)$. [6+4]

- 11.a) Write a short notes on Programmable array Logic.
b) Design a combinational circuit using ROM. The circuit accepts a four bit number and outputs a binary number equal to the square of the input number. [4+6]

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